Results in Physics 7 (2017) 1389–1395

Contents lists available at ScienceDirect

Results in Physics

journal homepage: www.journals.elsevier.com/results-in-physics

Towards coplanar quantum-dot cellular automata adders based on efficient three-input XOR gate

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ARTICLE INFO

Article history:
Received 3 March 2017
Accepted 6 April 2017
Available online 10 April 2017

Keywords:
Quantum-dot cellular automata
XOR gate
Full adder
Ripple Carry Adder
Nano technology
Coplanar

ABSTRACT

Quantum-dot cellular automata (QCA), which is a candidate technology to replace CMOS technology, promises extra low-power, extremely dense and high-speed structures at a nano scale. In this paper, a novel 3-input XOR gate structure is proposed based on half distance and cell interaction. Accordingly, a low-complexity and high-speed QCA one-bit full adder is designed by employing the proposed 3-input QCA XOR gate. Then a new 4-bit QCA Ripple Carry Adder (RCA) is proposed based on the proposed 3-input QCA XOR gate. The proposed designs are simulated using the both coherence and bi-stable simulation engines of QCADesigner version 2.0.3. Our simulation results indicate the efficiency and robustness of the proposed designs. The simulation results show 50% area improvement for the proposed 3-input XOR gate, 76% and 50% improvements in terms of cell count and latency, respectively for the proposed robust QCA full-adder, 58% and 52% improvements in terms of latency and cost, respectively for 4-bit QCA RCA compared to the previous designs.

Introduction

The conventional technologies such as CMOS technology have faced with problems such as high-noise absorption, high-power consumption, short circuit effects [1], and reducing gate control [2]. As a result, the possibility of constructing VLSI with low-power consumption, high-speed, high-density and easily build has become more difficult. Thus, the researchers are required to use the substitute technologies. Single electron transistors [3], molecular devices [4], Spintronics [5], Quantum-dot cellular automata (QCA) [1,6,7] and Carbon-Nano-Tube Field Effect Transistors (CNTFETs) [8,9] are considered as replaced technologies [10,11]. Based on three criteria power, area and delay time, QCA can be considered as an alternative for CMOS technology.

In this paper, we propose an efficient 3-input QCA XOR gate using explicit interactions between QCA cells. In addition, we have use a half distance. To show the suitable functionality of the proposed XOR gate, a one-bit full adder and a 4-bit QCA Ripple Carry Adder (RCA) is constructed based on the proposed QCA XOR gate. The proposed architectures are simulated using QCADesigner. The simulation results show that the proposed architectures have advantages compared to other QCA architectures.

The rest of this paper is organized as follows. In Section "Back ground", an over view of the QCA and related works are presented. A novel 3-input QCA XOR gate is proposed in Section "The proposed architectures". In addition, we construct a new QCA one-bit full adder cell and a new 4-bit RCA based on this novel XOR gate. Section "Simulation and Comparison Results" compares the proposed architectures to other QCA architectures. Finally, Sectio n "Conclusion" concludes this paper.

Back ground

Quantum cells

Quantum cells are tunneling elements that act on the transaction and interaction between quantum dots. Quantum cells form as square blocks that are two electrons within them. Unlike conventional structures, the logical values in this structure are not displayed using voltage levels, but they are determined according to the position of electrons in quantum dots. This notion was proposed in 1993 by Lent et al. [6]. Using QCA, the chip area and power

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http://dx.doi.org/10.1016/j.rinp.2017.04.005
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consumption are significantly reduced and the operating frequency are considerably increased. Fig. 1 shows a simplified quantum cell.

As it is shown in Fig. 1, a square space with two free electrons constitute quantum cell. There is a point in every corner called quantum dots. Electron pairs in each cell can move by the tunneling quantum dots, but due to coulomb interaction between them, that are always located in diameter, position of electrons in the cell determines the cell polarity. This polarization has two values +1 and −1, which are interpreted in binary logic one and zero. So, if one cell with polarity +1 is placed near other cells, due to the repulsion between the electrons of two adjacent cells, the cell polarity also changes to +1.

QCA contact wires

Fig. 2 shows wire crossing methods in the QCA technology.

In this technology, wires which are formed from the same quantum cells, interact with each other to transmit information. This means that the polarization of adjacent cells is transmitted along the wire due to coulomb interactions.

QCA gates review

Using the displacement cells and create new layout, the main gates of the QCA technology are constructed. Inverter gate and majority gate are two main gates in this technology. Figs. 3 and 4 show three types of inverter and two types of 3-input majority gate, respectively.

The majority gate is one of the most important gates in the QCA technology, which has an important role in structure of circuits. The logical function of 3-input majority gate is as follows:

$$M(A,B,C) = AB + AC + BC \tag{1}$$

In addition, 5-input majority gate is defined according to Eq. (2) and Fig. 5.

$$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \tag{2}$$

QCA clocking

QCA circuits use clock signals for transmission of signals. The clock signals control the QCA circuits without the need of power or signal wires.

However, the QCA system does not possess any external control on every cell compared to conventional CMOS circuits. QCA circuits are divided into four clock zones, which are 90° out of phase from each other. These four clock zones, which are shown in Fig. 6, are known as switch, hold, release and relax, respectively [17]. The cells are refreshed every clock cycle to synchronize and control information at each computational point.

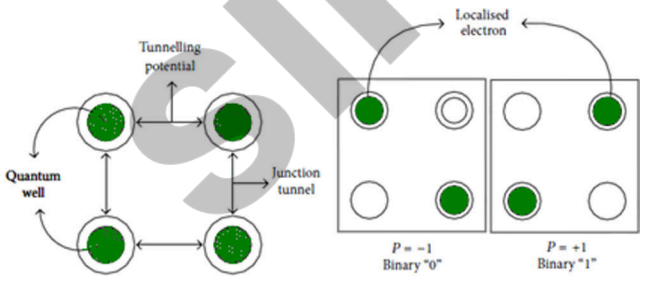

Fig. 1. The simplified quantum cell [12].

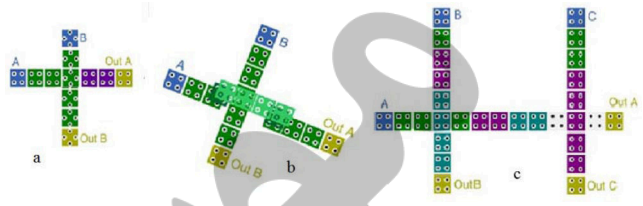

Fig. 2. Wire crossing methods: (a) single layer wire crossing, (b) multi-layer wire crossing, (c) logical crossing [13].

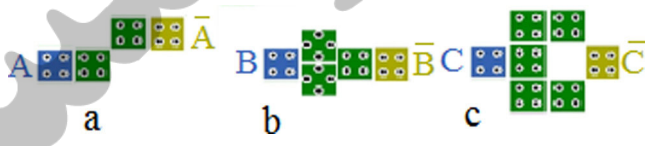

Fig. 3. Threetypesofinverter[14].

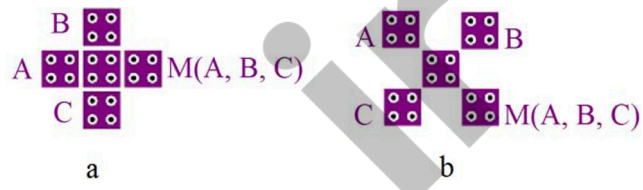

Fig. 4. Two types of 3-input majority gate [15].

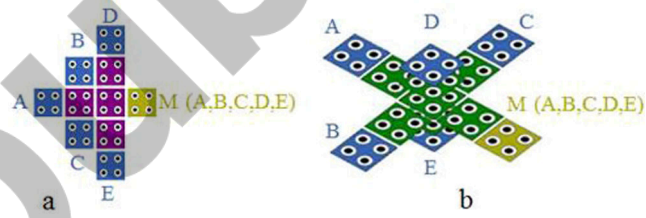

Fig. 5. Two types of 5-input majority gate, (a) single layer (b) multi-layer [16].

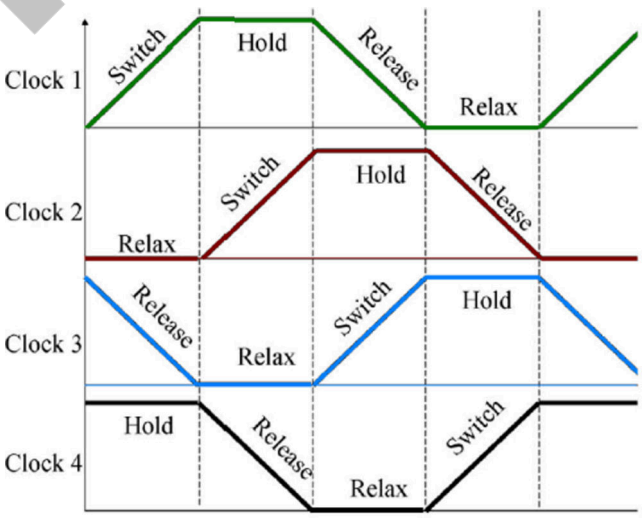

Fig. 6. Clock zones in QCA technology [18].

QCA XOR gate

Because of the significant application of XOR component in various works such as full adder designing, equality checking and detection and correction mechanism in the receiver and sender units, the implementation of efficient and high-speed XOR gate is one of the most important challenges in the QCA technology.

In the 2-input XOR gate with inputs A and B, the output is calculated as follows:

$$A \oplus B = \bar{A}B + A\bar{B} \tag{3}$$

The output of the 3-input XOR gate is also determined as follows:

$$A \oplus B \oplus C = ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} \tag{4}$$

QCA full adder

In the full adder with inputs A, B and C, the outputs of sum and $Carry_{out}$ are calculated as follows:

$$Carry_{out} = AB + BC_{in} + AC_{in} \tag{5}$$

$$Sum = A \oplus B \oplus C_{in} = ABC_{in} + \bar{A}\bar{B}C_{in} + A\bar{B}\bar{C_{in}} + \bar{A}B\bar{C_{in}} \tag{6}$$

To design the full adder in the QCA technology, $Carry_{out}$ can be reformulated as follows:

$$Carry_{out} = M(A, B, C_{in}) \tag{7}$$

where $M(A, B, C_{in})$ denotes a 3-input majority gate.

In addition, sum can be reformulated as follows:

$$\begin{aligned} Sum &= M(\overline{Carry_{out}}, M(A, B, \overline{Carry_{out}}), C_{in}) \\ &= M(\overline{Carry_{out}}, M(A, B, \overline{Carry_{out}}), B) \\ &= M(\overline{Carry_{out}}, M(A, B, \overline{Carry_{out}}), A) \\ &= M(\overline{Carry_{out}}, \overline{Carry_{out}}), C_{in}, A, B) \end{aligned} \tag{8}$$

Which can be implemented using 5-input majority gate. As a result, efficient implementation of 3-input XOR gate and 5-input majority gate can improve the full adder implementation.

Previously reported designs

A XOR gate is one of the most important gates in the QCA technology. Figs. 7 and 8 show the 2-input and 3-input QCA XOR gates [19,20,21].

The 3-input XOR gate is usually designed using 2-input XOR gates. In this method, the QCA implementation of 2-input XOR gate has a crucial role in the circuit performance [19,20,14].

The authors of [21,22] have proposed 3-input QCA XOR using two majority gates (3-input and 5-input majority gates) as shown in Figs. 8 and 9. According to the identical latency of multi-input

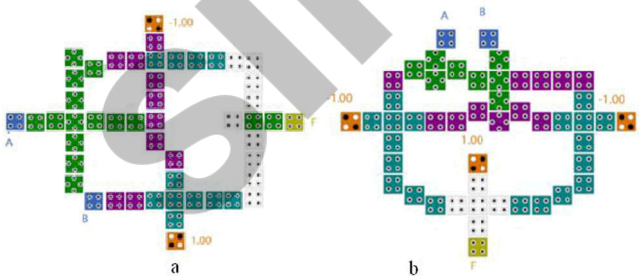

Fig. 7. The 2-input QCA XOR gate: (a) in [19], (b) in [20].

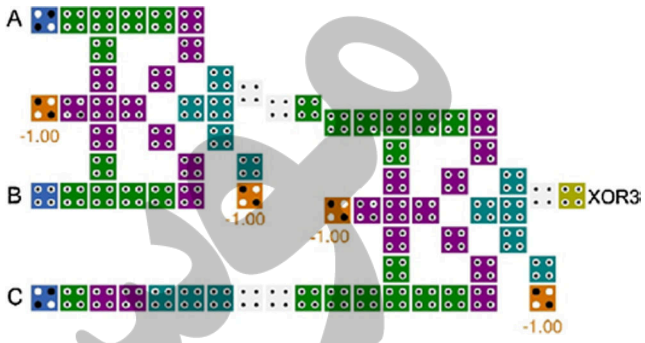

Fig. 8. Conventional implementation of a 3-input QCA XOR gate using 2-input QCA XOR gates based on the module in [21].

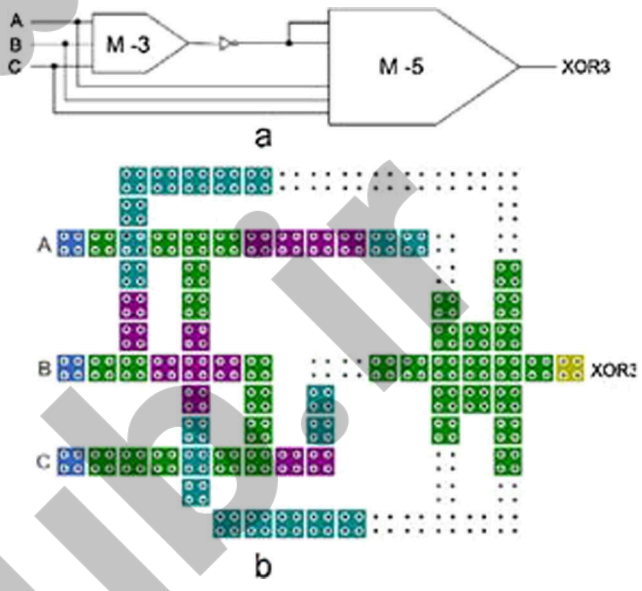

Fig. 9. The 3-input QCA XOR gate in [22] (a) logical diagram (b) QCA layout.

majority gates, this reducing gate level design can improve the performance of QCA XOR gate [22].

Firdous Ahmad et al. [23] presents a 3-input QCA XOR, which is shown in Fig. 10. The structure of this design is different from previous designs and it is not based on the majority gates.

As it is mention in the previous section, the QCA full adder structure can be implemented using QCA XOR gate. For example, the authors of [24] have proposed QCA coplanar full adder using 59 cells as shown in Fig. 11.

In this full adder, the latency is 1 clock cycle, and the area is 0.043 μm^2.

The proposed architectures

This section presents a novel QCA XOR gate. Then, a novel full adder and RCA architectures are presented based on this novel QCA XOR gate.

The proposed efficient 3-input QCA XOR gate

Fig. 12 shows the proposed 3-input QCA XOR gate. Our proposed 3-input XOR gate uses explicit interactions and half space between QCA cells.

As illustrated in Fig. 12, the proposed 3-input QCA XOR architecture only consist of a 5-input majority with 14 QCA cells. The area of the proposed 3-input QCA XOR gate is 0.01 μm^2.

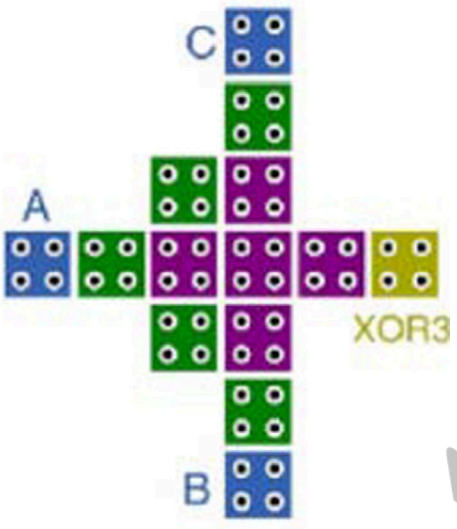

Fig. 10. The presented 3-input XOR gate in [23].

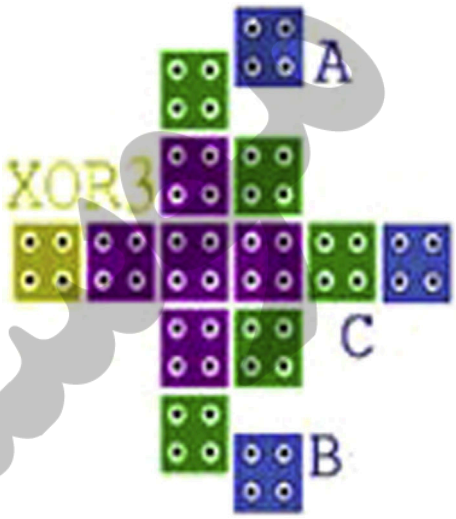

Fig. 12. The proposed 3-input XOR gate.

It should be noted that, by fixing each of the three inputs in the proposed explicit interaction of 3-input QCA XOR to 0 or 1, 2-input XOR or XNOR gates can be accomplished, respectively.

The proposed QCA full adder architecture

In this section, a robust QCA full-adder is presented using the proposed 3-input QCA XOR gate. Fig. 13 demonstrates the structure of the proposed QCA full adder architecture.

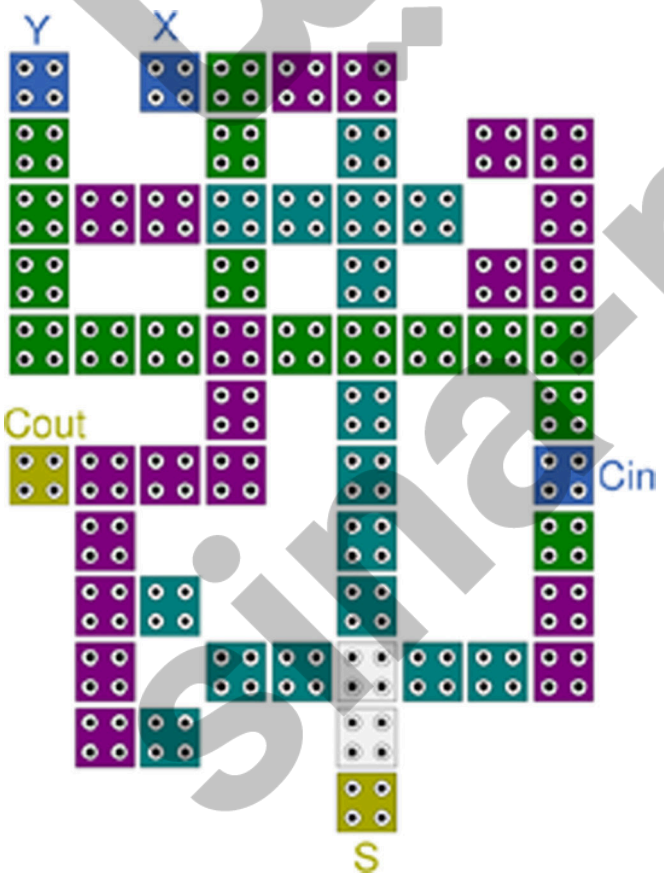

Fig. 11. The QCA full adder layout in [24].

As it is shown in this figure, the carry is produced by the 3-input majority gate and the sum is produced using the proposed 3-input QCA XOR.

The proposed 4-bit RCA

Fig. 14 shows the proposed 4-bit QCA RCA architecture, which is utilized the proposed 3-input QCA XOR gate as its structured unit. The proposed 4-bit RCA is consists of 29 cells, which has a 0.02 μm^2 area. So, the cells are also located in four clock zones.

Simulation and comparison results

In this section, the cost value is determined using the following equation:

$$\text{Cost} = \text{Area} * \text{Latency} \quad (9)$$

where Area is shown in terms of μm^2 and Latency denotes the number of clock cycles.

The proposed 3-input QCA XOR gate

Fig. 15 shows the simulation results for the proposed 3-input QCA XOR gate in QCADesigner.

As it is shown in the achieved simulation waveform in Fig. 15, the circuit performs correctly. However, the latency is 0.5 clock cycles.

Table 1 shows the comparison of the proposed 3-input QCA XOR gate with other 3-input QCA XOR gates in [21,23,24] which are designed in single layer.

According to Table 1, the proposed 3-input QCA XOR gate has 85%, 84%, 60%, and 94% improvements in terms of area occupation, cell count, circuit latency and cost, respectively in comparison to [21]. Despite similar area to that of the design presented in [23], our proposed design surpasses it by 50% improvements in terms of area and cost.

The proposed QCA full adder architecture

Fig. 16 shows the simulation results for the proposed QCA full adder.

As it is shown in the achieved simulation waveform in Fig. 16, the proposed circuit for the QCA full adder performs correctly.

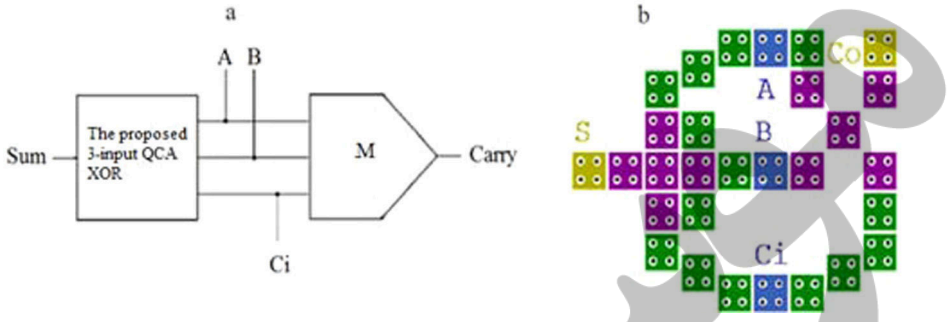

Fig. 13. The proposed robust QCA full-adder (a) logical diagram, (b) QCA layout.

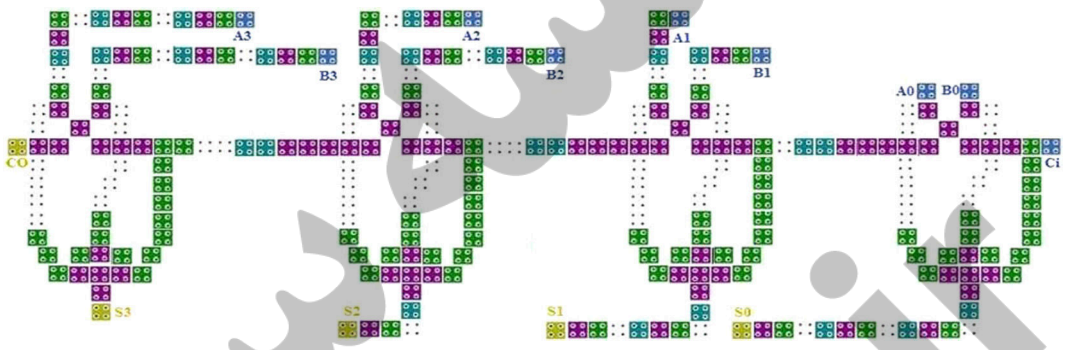

Fig. 14. The layout of the proposed 4-bit QCA RCA.

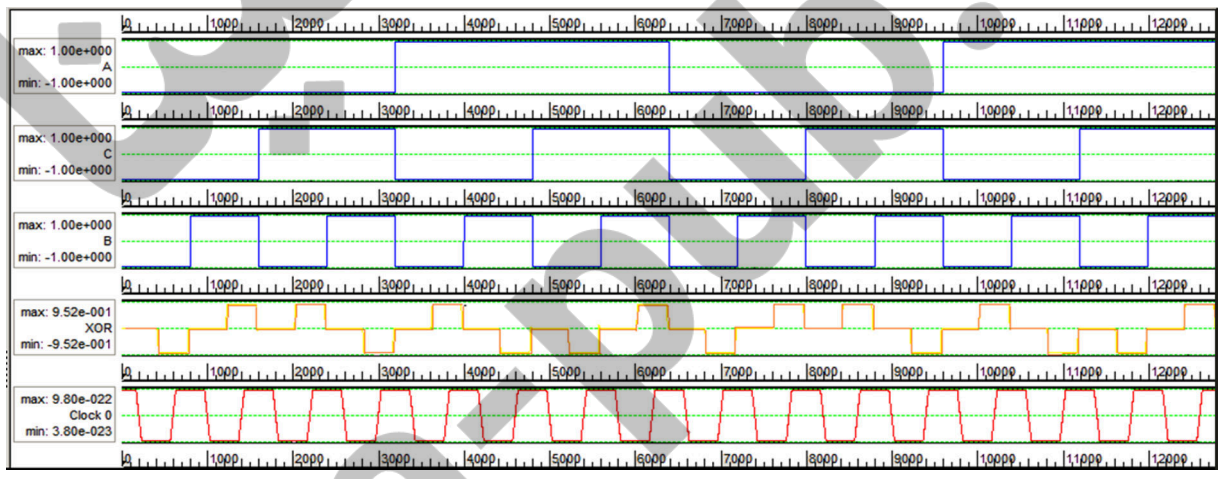

Fig. 15. The simulation results for the proposed 3-input XOR.

Table 1
Comparison table for the single layer 3-input QCA XOR gates.

Refs.	Area (μm^2)	Gate count	Cell count	Latency (clock cycle)	Cost
[21]	0.08	2	75	2	0.16
[23]	0.07	3	93	1.25	0.0875
[24]	0.02	1	14	0.5	0.01
This paper	0.01	1	14	0.5	0.005

Table 2 shows the extensive comparison of the proposed QCA full adder with other full adders in [21,23–29].

According to Table 2, our proposed design achieved the best results in comparison with other QCA full adder circuits in terms of area occupation, cell count, circuit latency and cost. In particular, the cell count, area, and cost of the proposed full adder are reduced by about 29%, 50%, and 50% in comparison with QCA full adder in [23].

Despite similar area to that of the multilayer design presented in [25], our proposed design surpasses it by 23%, 83%, and 83% improvements in terms of cell count, latency and cost, respectively.

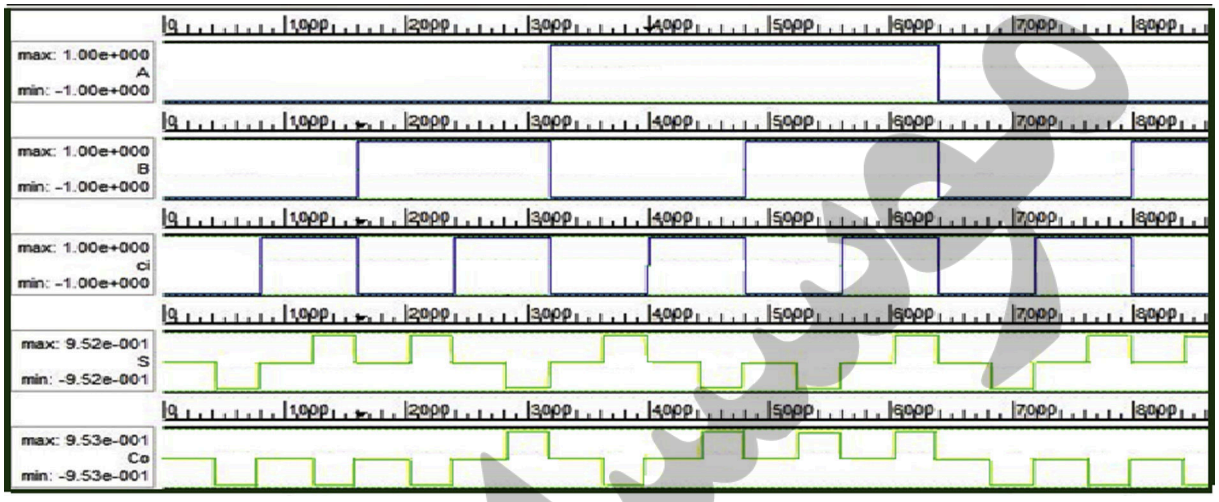

Fig. 16. The simulation results for the proposed full adder.

Table 2
Comparison table for the QCA full adders.

Refs.	Cell count	Area (μm2)	Latency (clock cycle)	Cross-over type	Cost
[26]	48	0.05	3	Coplanar	0.15
[25]	38	0.02	3	Multilayer	0.06
[21]	95	0.09	1.25	Coplanar	0.1125
[24]	59	0.043	1	Coplanar	0.043
[27]	49	0.04	1	Coplanar	0.04
[28]	52	0.04	0.75	Multilayer	0.03
[29]	51	0.03	0.75	Multilayer	0.0225
[23]	41	0.04	0.5	Coplanar	0.02
This paper	29	0.02	0.5	Coplanar	0.01

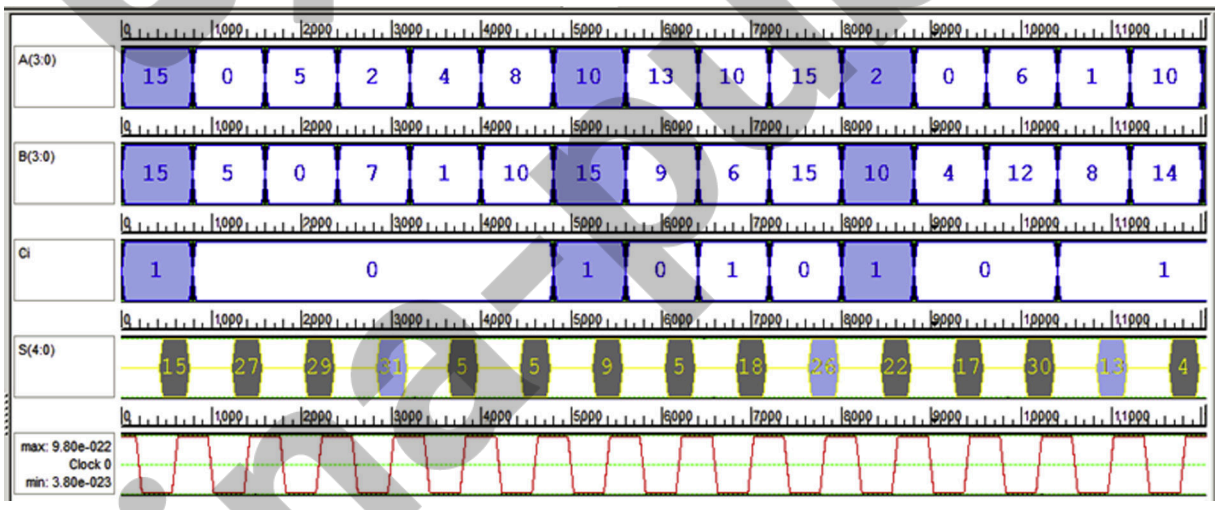

Fig. 17. The Simulation results for the proposed 4-bit RCA.

Table 3
Comparison table for the QCA 4-bit RCA.

Refs.	Cell count	Area (μm^2)	Latency (clock cycle)	Cross-over type	Cost
[30]	651	1.2	17	Coplanar	20.4
[29]	308	0.29	8	Coplanar	2.32
[24]	262	0.208	7	Coplanar	1.456
[25]	237	0.24	6	Multilayer	1.44
This paper	269	0.37	3.5	Coplanar	1.295

In addition, our simulation results show that the proposed QCA full adder provides an improvement in terms of area occupation, cell count, circuit latency and cost in comparison with other QCA full adder circuits in [28,29], which is implemented in single layer. However it is also competitive with multilayer designs.

The proposed 4-bit RCA

The simulation results of the proposed 4-bit RCA are shown in Fig. 17.

According to Fig. 17, after 3.5 clock phase delay, the sum of the inputs (A, B, C_{in}) is calculated, which is absolutely corrected.

Table 3 contains a comparison between our proposed 4-bit QCA RCA and other 4-bit QCA RCA architectures.

Based on our simulation results, which are shown in Table 3, the proposed design has the lowest circuit latency and cost compared to other QCA RCA designs in [24,25,29,30].

In particular, despite the lower number of cells in [25], our proposed design has 41% and 11% improvements in terms of latency and cost, respectively. It should be noted that Ref. [25] has been a multi-layer design.

As it is shown in Table 3, the proposed structure in Fig. 14 virtually excels all the counterparts with a considerable superiority. The cell count, circuit latency and cost of the proposed 4-bit RCA architecture are 13%, 56%, and 44% less than that of [29], respectively.

Conclusion

The QCA is an alternative for CMOS technology at Nano-scale level due to its small size, very high switching speed and ultra-low power consumption. On the other hand, XOR gate is one of the most important gates in digital circuits such as full adders. In this paper, a novel QCA structure was proposed for 3-input QCA XOR, which is based on the half distance. Using the proposed QCA XOR gate as the main building block, a novel QCA structure was presented for full adder. We also used this new 3-input XOR to design a robust and efficient 4-bit RCA in the QCA technology. The proposed designs were implemented using QCADesigner version 2.0.3. Our simulation results showed that our proposed designs have yielded significant improvement in term of cost.

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